IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of

GILKERSON — Atty. Ref.: SCS-550-525

Serial No. 10/779,808 — TC/A.U.: 2183

Filed: February 18, 2004 — Examiner: R. Fennema

For: DETERMINING TARGET ADDRESSES FOR INSTRUCTION FLOW CHANGING INSTRUCTIONS IN A DATA PROCESSING APPARATUS

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October 19, 2007

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

REPLY BRIEF

This Reply Brief is responsive to the Examiner's Answer mailed August 21, 2007 and the various new points of argument made in the "Response to Argument" portion of the Examiner's Answer, i.e., Sections 25-30.

Prior to pointing out the defects in each of the Examiner's responses to the Appeal Brief Sections A-F, it may be more helpful for Appellant to again reiterate the operation of Appellant's claimed invention, especially with respect to the prior art cited by the Examiner.

The central difference between the present invention and the prior art cited by the Examiner is the provision of asymmetric address generation paths in the prefetch unit of the present invention. The first attachment to this Reply Brief comprises a double copy

of Figure 1 in which the upper copy highlights the first address generation path and in the lower copy the second address generation path is highlighted.

As is set out in Appellant's independent claims, the inventive idea is that, if a selected prefetched instruction is detected to be an instruction flow changing instruction (IFCI), then one address generation path or the other is used, i.e. as claimed, the "quicker" first address generation path is used if the selected instruction is the first prefetched instruction and the "slower" second address generation path is used if the selected instruction is anything other than the first prefetched instruction.

Thus, as noted above, the upper highlighted version of Figure 1 discloses the first address generation path detected to be an IFCI and in the lower Figure 1 the slower address generation path is used if the instruction is anything other than the first prefetched instruction. The manner in which the first address generation path is made quicker is also set forth in the last paragraph of Appellant's claim 1 (the inclusion of "a pipeline stage, provided in said at least one further address generation path, for increasing generational speed of the target address . . . .").

As discussed on page 14, lines 21-23 of the present specification, for the "first address generation path" the target address is calculated in one cycle, i.e., directly from decode logic to the multiplexer 85 as shown in the upper Figure 1. However, for the relatively slower "at least one further address generation path," it can be seen that the logic flow is through offset multiplexer 80 and the offset register 82. As disclosed in the above-referenced portion of the specification, for the upper Figure 1 the target address is

calculated in one cycle while for the second group the target address is calculated in two cycles due to the presence of the offset register 82.

The above language is also specifically recited in Appellant's independent claims as "a pipeline stage, provided in said at least one further address generation path, for increasing generation speed of the target address by the first address generation path." As will be clearly understood, the addition of the pipeline stage in the at least one further address generation path (shown in the lower Figure 1 of the attachment) will make address generation slower in the lower one or, relatively speaking, faster in the upper one.

Appellant also encloses herewith a handwritten schematic of the disclosure which appears to be relied upon by the Examiner in the Furber reference. Furber describes a branch prediction unit which on page 387 (last two lines) is said to work like the jump trace buffer described on page 382 (see the last paragraph). However, the branch prediction unit is stated as having two 8-entry halves, as noted by the Examiner, at Furber page 388. This is shown in the attached figure.

It is clear from what is described in Furber that both instructions are passed to the branch prediction unit (whether they are IFCIs or not) and the branch prediction unit works out for each one whether it is an IFCI and, if so, what the target address is. If both of Furber's instructions are IFCIs, then both target addresses are clearly output by the lookup structure of the branch prediction unit **at the same time** and this is what gives rise to the "hit in both halves" mentioned on page 388.

As stated on page 388 of Furber, in such a situation (where there is a "hit in both halves"), the target of the first instruction "(at the even address)" is given priority. This

emphasizes that both target addresses have been generated by that time. Indeed, if they had not, there would certainly be no need to award priority to one of them.

The present invention and Furber do have one similarity and that is, if there is more than one IFCI in a block of prefetched instructions, it is the branch address for the first appearing IFCI that is relevant, since that is the one that will cause a branch to take place. As a result, the branch defined by the later appearing IFCI in the block of prefetched instructions will not be relevant, since that instruction will not be executed. From the Examiner's underlined comments on page 18 of the Examiner's Answer, he has clearly misunderstood this point.

As will be seen by the detailed response to the Examiner's comments on the misunderstood Furber reference, there is no disclosure of a quicker path as a result of an increased generation speed of either address generation path disclosed.

A. Examiner's response to Appeal Brief Section A. "The Furber prior art, where there is an instruction flow changing instruction [IFCI], does not teach a determination between two address generation paths based upon the IFCI being a first prefetched instruction"

On page 17 of the Examiner's Answer, the Examiner suggests that he treats a branch instruction as an IFCI (and this appears to be supported by Appellant's specification as filed, page 1, lines 14-18). However, in response to Appellant's request that the Examiner point out where Furber teaches a determination that an instruction is an IFCI, i.e., an instruction flow changing instruction, the Examiner curiously states as support "Zero comes before One, Two comes before Three." (Examiner's Answer, Section 25, line 9). Thus, according to the Examiner's own understanding of the Furber

reference, "zero" and "two" would be handled by the "even" half of the branch prediction unit and "one" and "three" would be handled by the "odd" half. The Examiner's interpretation is clearly contrasted with the language of claim 1 which requires that "a first address generation path" is used if the selected prefetched instruction is a "first prefetched instruction", i.e., the path shown in the upper Figure 1 of the attachment and the "at least one further address generation path" is used if the selected prefetched instruction is one of the "other prefetched instructions."

Thus, using the Examiner's logic and the present claim 1, only "zero" would be handled by the first path (on the "even" side of Furber) and "one," "two" and "three" would be handled by the second path (on the "odd" side of Furber). Not only does Furber not disclose such handling as claimed in Appellant's independent claims (the "zero' corresponds to the "first address generation path" and "one," "two," and "three" correspond to the "further address generation path[s]"), but Furber, as acknowledged by the Examiner, clearly teaches away from the first instruction being handled by one path and all other instructions handled by the second path.

In the Appeal Brief, appellant specifically requested the Examiner to identify three features set out in Appellant's claims (i.e., "where there are at least two separate address generation paths and, even more specifically, where there is any determination in Furber as to whether the selected instructions is an IFCI and if an IFCI whether it is 'said first prefetched instruction'." Appeal Brief, paragraph bridging pages 13 and 14). To the extent the Examiner actually does believe the Furber branch prediction unit has two

paths, i.e., the "even" and the "odd" half, he has arguably disclosed the first of the features.

However, the Examiner does not identify where there is any determination in Furber as to whether the selected instruction is an instruction flow changing instruction, nor is there any determination of whether it is the "first prefetched instruction." Instead, Furber clearly teaches that the instructions enter each half of the branch prediction unit at the same time and pass through each unit in the same period of time. This is readily apparent because the system is wired so that "the target of the first instruction (at the even address) takes priority," i.e., when hits occur in both halves there must be a priority arrangement to break the "tie." The Examiner's failure to identify where all three features exist in the Furber reference proves the impossibility of his obviousness argument.

As noted above, Furber specifically teaches away from the claimed structure of having a first address generation path in the event of a first prefetched instruction and a further address generation path in the event of "the other prefetched instructions." Using the Examiner's number analogy, the claim is tantamount to having the "zero" instruction handled in the "even" half (i.e., the first path) and all others being handled in the "odd" half (i.e., the second path). Of course, Furber doesn't teach this and instead merely teaches splitting between "odd" and "even" numbered instructions and therefore clearly leads one of ordinary skill in the art away from Appellant's claimed address generation logic.

B. Examiner's response to Appeal Brief Section B. The Furber reference does not teach "the first address generation path generating the target address more quickly than the at least one further address generation path"

Beginning on page 18 of the Examiner's Answer, the Examiner contends that the choosing of "priority" in the Furber reference is a disclosure of the claimed "the first address generation path generating the target address **more quickly** than the at least one further address generation path" recited in Appellant's independent claims (emphasis added). The Examiner provides no support for this contention and appears to ignore the fact that Furber specifically states that "a packet with a branch in each half word may 'hit' in both halves, whereupon the target of the first instruction (at the even address) takes priority." Quite clearly, the "hits" occur and pass through each of the halves at the same speed, and, as a result, require an instruction to take the "target of the first instruction (at the even address)" as having priority to break the tie.

Thus, as can clearly be understood, "priority" as used in Furber does not mean "more quickly" and instead just means that, in the choice between two available options, one is given "priority." It says nothing about one choice being received more quickly than the other and logically, there would be no need to prioritize if they had different generation speeds.

Moreover, as set out in the second full paragraph of the Appeal Brief at page 15, the Examiner has not retracted or modified his previous admission, i.e., that Furber fails to teach "a pipeline stage, provided in said one further address generation path, for increasing generation speed of the target address by the first address generation path."

Because the Examiner has admitted this interrelationship and it is clear that Appellant's claim requires "the first address generation path generating the target address more quickly than the at least one further address generation path," the burden is on the Examiner to explain this error.

The Examiner expends almost two pages in the Examiner's Answer (pages 18 and 19) attempting to establish that "priority" of choice is the same thing as faster or slower address generation speed, but provides no supporting logic. The fact is that Furber does not contain any disclosure suggesting that one path through the branch prediction unit is faster than alleged path.

More significantly, Appellant's independent claims specify the pipeline stage "provided in said at least one further address generation path" for increasing generation speed of the target address by the first address generation path. As discussed above, this is the offset multiplexer 80 and the offset register 82 which serves to slow down the at least one further address generation path, thereby, relatively, speeding up the first address generation path as required by the claim.

The Examiner appears to ignore this specific structure recited in Appellant's apparatus, method and logic claims. Accordingly, even if the Examiner was correct and there was somehow a difference in speed through the odd and even halves of the Furber branch prediction unit as he contends, there is no specific structure (the claimed "pipeline stage"), method step or logic meeting the limitations of Appellant's independent claims 1, 11 and 21, respectively. Therefore, Furber not only fails to disclose, but actually teaches away from Appellant's claimed combination.

C. Examiner's response to Appeal Brief Section C. The Patterson reference is not alleged to disclose the above two features clearly missing from the Furber reference

In response to Appellant's challenge for the Examiner to "cite the portion of Patterson relied upon for this claim teaching" (the teaching of the claimed "determining" between the two paths and the "more quickly" caused by the "pipeline stage") as noted in the Appeal Brief, last full paragraph on page 16 and in the paragraph bridging pages 16 and 17), the Examiner fails to make any response.

However, the Examiner does allege that these are claim limitations "that are not present in the claims, namely, deciding between two paths." (Examiner's Answer, page 20, lines 1-2). Again, the Examiner is clearly erroneous in his conclusion. One only need look at the "address generation logic" in claims 1, 11 and 21 which states "for determining a target address to be output." This "determining" step makes the decision between the "first address generation path" and "at least one further address generation path" as clearly set forth in the claim.

Thus, the Examiner's conclusion that the claim does not make a determination between the two paths is simply erroneous. If the Examiner is placing some criticality on the word "deciding" which is not used in the claim and "determining" which is actually used in the claim, he is attempting only to create a straw-man argument and is ignoring the language of Appellant's claims.

Furthermore, rather than address the issue of the Patterson reference disclosing nothing which is pertinent to the claimed invention, the Examiner merely addresses Patterson by saying that "the fact that Furber or Patterson allegedly do not teach these

features is immaterial." (Last line of Section 27 in the Examiner's Answer). The Examiner's ignoring of written claim limitations and the Appeal Brief's challenges to point out where those claim limitations exist in the prior art is fatal to any alleged *prima facie* case of obviousness.

D. Examiner's response to Appeal Brief Section D. The combination of the Furber and Patterson references fails to teach the claimed invention

In Appellant's Appeal Brief on page 17, it is pointed out that based upon the previous discussions in Sections A-C, it is clear that the Furber and Patterson references both fail to teach at least one structure recited in Appellant's independent claims. The point is that, if neither of these two claimed structures is disclosed in either Furber or Patterson, even if these prior art references were combined, they can't render obvious the subject matter of the independent claims.

The Examiner provides no response to this and merely refers to his previous remarks regarding the Furber and Patterson references. As has been demonstrated above, because neither Furber nor Patterson disclose the subject matter of the claimed invention, the combination of these references cannot disclose that claimed subject matter.

E. Examiner's response to Appeal Brief Section E. The Examiner fails to identify any "reason" or "motivation" for combining the Furber and Patterson references

On page 20 of the Examiner's Answer, it is suggested that the basic improvement of "pipelining" is beneficial and therefore this is the "reason" or "motivation" for combining the two references. The Examiner misses the point of the Federal Circuit's

decisions relating to combining references that the "reason" must be a reason for picking and choosing elements from the different references and then combining them in the manner set out in the claims. Merely suggesting that pipelining provides a speed benefit and thus one would somehow be motivated to pick and choose elements from the two references and combine them in the manner of Appellant's claims is simply insufficient.

Also, it is noted that there is a certain additional amount of processing time required for each pipeline stage and, as noted above, it is the addition of "a pipeline stage" (as shown in the lower Figure 1 of the attachment) that actually slows the generation of target addresses in the at least one further address generation path. Thus, the claimed "pipeline stage" (see items 80 and 82 in the lower Figure 1 in the attachment) is actually used to slow down address generation for the further address generation paths, making the first address generation path relatively faster.

Additionally, the Examiner seems to rely upon a misunderstanding of the Supreme Court decision in *KSR* as somehow obviating the need to provide a proper "reason" for combining references. The Examiner's attention is directed to the Memorandum issued May 3, 2007 by Deputy Commissioner for Patent Operations, Margaret A. Focarino, in which she provided the Patent Office position regarding the Supreme Court decision in *KSR*. It is the Court's position that "to facilitate review, this analysis [by the examiner] should be made explicit." The Deputy Commissioner held that "therefore, in formulating a rejection under 35 USC §103(a) based upon a combination of prior art elements, it remains necessary [for the examiner] to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed."

The Examiner, as noted in the Appeal Brief, simply has failed to meet his burden of establishing some "reason" or "motivation" for combining elements of the two references (even assuming that those elements are disclosed in at least one of the two references).

F. Examiner's response to Appeal Brief Section F. The Examiner fails to appreciate that Furber would lead those of ordinary skill in the art away from the claimed invention

On page 21 of the Examiner's Answer, the Examiner provides no argument or dispute with respect to the fact that Furber's teaching of equally speedy address generation paths which requires priority to be given to the "even" address path (Furber at 388), clearly leads one of ordinary skill in the art from having two different speed address generation paths. If Furber had any difference in his address generation paths, he would not need to give priority to the "even address path."

The only argument the Examiner does make is the rather foolish statement that "it is quite impossible for Furber to teach away from the invention when Furber himself teaches the invention." As noted above, it is clear that Furber does not teach two claimed aspects of Appellant's invention (the two paths, one for only the first address generation path and the other for all other generations paths and the "more quickly"). Instead, Furber teaches the need for a priority determination to be made when, as is always the case in Furber, two hits arrive in both halves together, priority is given to the first instruction "at the even address." With the lack of any difference in address generation

speed, Furber quite clearly teaches away from Appellant's claimed invention, thereby indicating the non-obviousness of the pending claims.

It is respectfully requested that the Board carefully consider the Examiner's "Response to Argument" portion of the Answer and the Examiner's lack of any identification of portions of either Furber or Patterson teaching two claimed features of Appellant's invention, i.e., (1) the address generation logic which has a first address generation path for a first prefetched instruction and at least one further address generation path for other prefetched instructions; and (2) the first address generation path generating the target address more quickly than the at least one further address generation path (as provided by the additionally claimed "pipeline stage").

Neither of these two structures is disclosed in either Furber or Patterson or any other prior art reference cited by the Examiner. As a result, not only is there no support for the claimed features, there is no support for the combination of references and in fact there is no substantive dispute as to the fact that Furber teaches away from the claimed invention.

As a result of the above, there is simply no support for the rejection of Appellant's independent claims or claims dependent thereon under 35 USC §103. Thus, and in view of the above, the rejection of claims 1-21 under 35 USC §103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

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Attachments:
Figure 1 double copy
Handwritten schematic

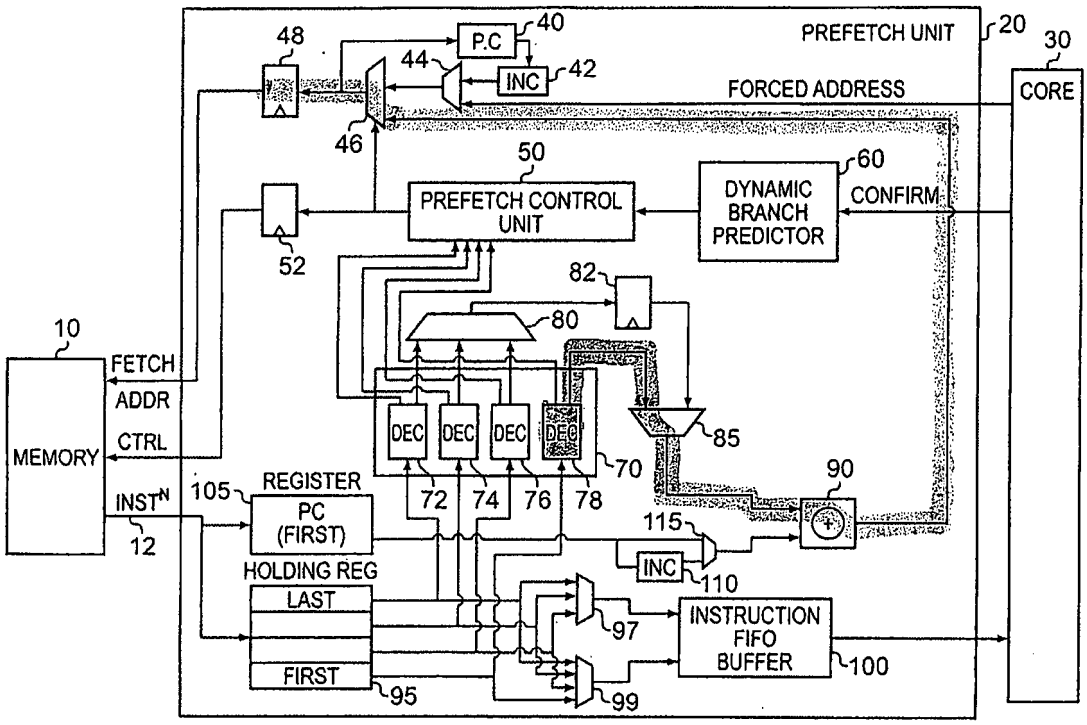

Fig. 1

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14 JUL 2006

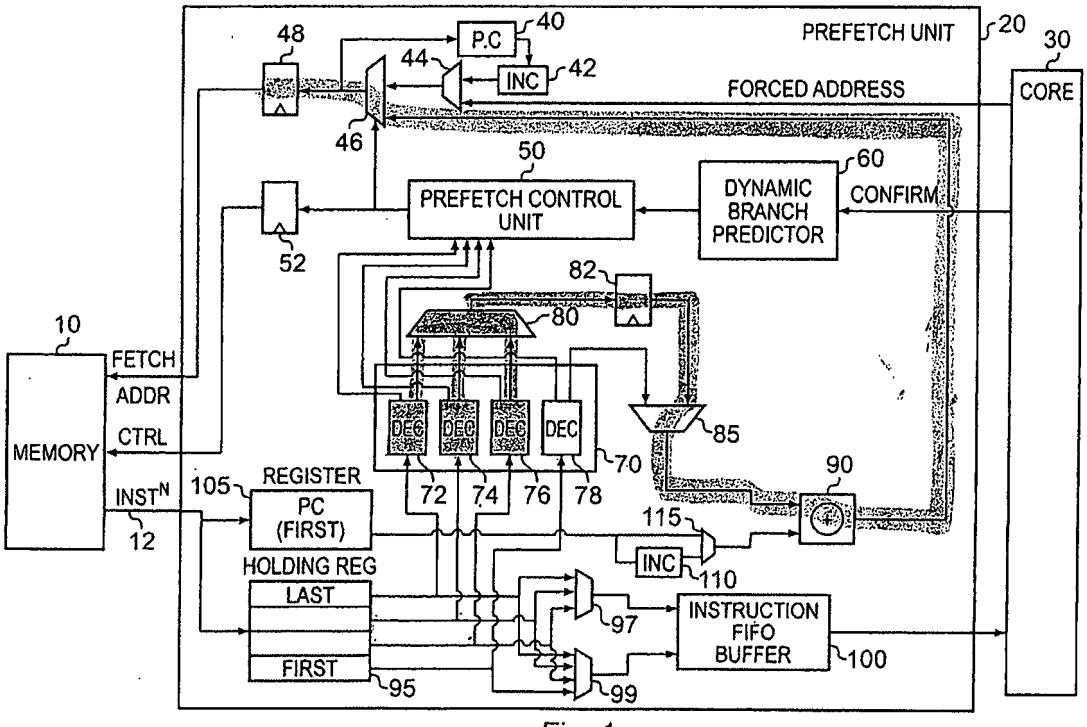

Fig. 1

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